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(54) Microcomputer with debugging system

(57) A microcomputer includes an internal memory, CPU core, bus controller, and debugging controller. The internal memory stores a control program. The CPU core executes the control program. The CPU core outputs a control signal made up of connection information containing the storage address of the control program and the address of the internal memory generated as a result of executing the control program, the instruction contents of the control program, and data generated by executing the control program. The bus controller controls signal exchange based on the operation of the CPU core via an address bus and data bus that are connected to an external memory. The bus controller has a data I/O controller for outputting an address obtained from the connection information in the control signal to the external address bus, and outputting the data in the control signal to the external data bus. The debugging controller generates trace information necessary for debugging operation for confirming an operation by the control program. The debugging controller has a trace information generator for extracting the instruction contents in the control signal as trace information, and a trace information output unit for externally outputting the trace information output from the trace information generator.

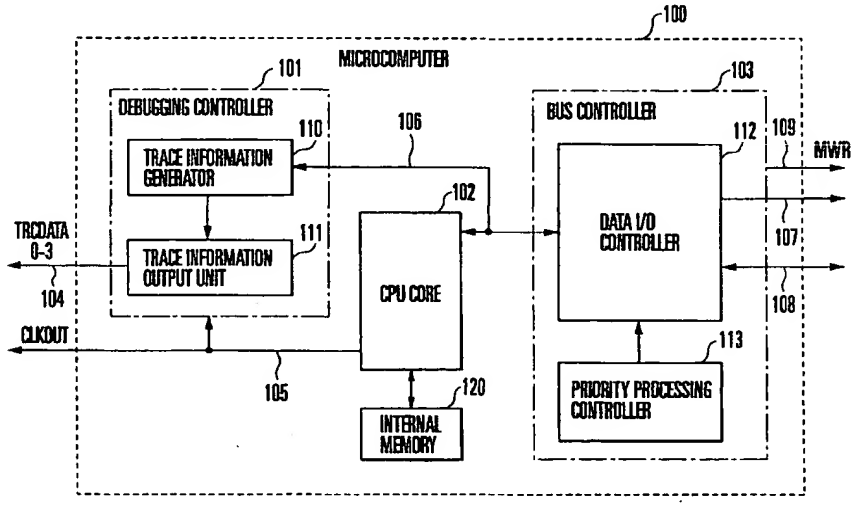

FIG. 1

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Description

Background of the Invention

[0001] The present invention relates to a microcomputer which has an on-chip debugging function and outputs access information to an external bus in accessing internal resources.

[0002] An increase in the speed of CPUs (Central Processing Units) and development in the type of CPU are remarkable. As a debugging environment coping with the speed, an on-chip debugging method of giving the CPU part of a debugging function is available. A conventional microcomputer incorporating the on-chip debugging function will be described with reference to Fig. 5.

[0003] In Fig. 5, a microcomputer 500 is constituted by a CPU core 502, bus controller 503, and debugging controller 501. The CPU core 502 performs control of generating and outputting a CLKOUT signal 505, and processing of outputting a control signal 506 and a branch destination address value to a PC trace bus 516 in executing a branch instruction generated when various instructions are executed.

[0004] The bus controller 503 comprises a data I/O controller 519 for performing I/O control based on the control signal 506 from the CPU core 502. The data I/O controller 519 exchanges an address value with an external address bus 507, exchanges data with an external data bus 508, and outputs write data to an emulation/data trace bus 517.

[0005] The debugging controller 501 comprises a trace information generator 514 for receiving signals on the PC trace bus 516 and emulation/data trace bus 517 and the control signal 506, and generating trace information, and a trace information output unit 515 for outputting trace information as a TRCDATA0-3 signal 518 in time division.

[0006] The trace information generator 514 generates trace information of a trace buffer overflow when the generator 514 receives the control signal 506 from the CPU core 502 as a result of executing a next instruction before the trace information output unit 515 outputs all trace information as the TRCDATA0-3 signal 518.

[0007] The trace packet format will be explained.

[0008] The trace packet is made up of 8 bits (format 1), as shown in Fig. 6A, or 40 bits (formats 2 and 3), as shown in Figs. 6B and 6C. In formats 1 to 3, lower four bits represent trace information. As the trace information, "0011" represents the overflow of the trace buffer, "0110" represents execution of a branch instruction, and "1001" represents execution of data access.

[0009] As shown in Fig. 6A, upper four bits in format 1 are fixed to "0000". As shown in Fig. 6B, upper four bits in format 2 represent the type of branch instruction. In this example, when an unconditional branch instruction is executed, "0100" is output.

[0010] As shown in Fig. 6C, bits 06 to 04 in format 3 represent the data access size, and "111" represents that access to one word (32 bits) has been executed. Bit 07 is fixed to "0". Bits 39 to 08 in format 2 shown in Fig. 6B represent a branch source address, whereas bits 39 to 08 in format 3 shown in Fig. 6C represent write data.

[0011] Trace information output operation of the debugging controller 501 will be described. In this case, the microcomputer 500 executes a branch instruction located at an address "OOOOOOH" in an internal memory (not shown) to branch to an address "000010H". Further, trace information is output as the TRCDATA0-3 signal 518 in executing an instruction located at an address "000010H" in the internal memory for write operation of 32-bit data "5A5A5A5AH" to an address "001000H" consecutively to the branch instruction.

[0012] In this example, the address bus width is 24 bits, the data bus width is 32 bits, and the internal buffer of the trace information output unit 515 is made up of 4 bits equal in number to the terminals of the trace information output unit 515.

[0013] To execute a branch instruction to the address "000010H" that is stored at the address "000000H" in the internal memory, the microcomputer 500 performs processing in the following order.

[0014] I) The CPU core 502 fetches the branch instruction from the address "OOOOOOH" in the internal memory, and executes the instruction. Then, the CPU core 502 outputs, to the bus controller 503 and debugging controller 501, the control signal 506 instructing output of the branch source address "000000H" to the external address bus 507. Further, the CPU core 502 outputs the branch source address "000010H" to the PC trace bus 516. These operations are access to the internal memory, so no data is output to the external address bus 507 and external data bus 508.

[0015] II) Upon reception of the control signal 506, the trace information generator 514 in the debugging controller 501 generates 40-bit trace data of format 2 (Fig. 6B), and outputs it to the trace information output unit 515. Based on this trace data, the trace information output unit 515 outputs a packet of format 2 (Fig. 6B) as the TRCDATA0-3 signal 518 (Figs. 7B to 7E) in synchronism with the leading edge of the CLKOUT signal 505 (Fig. 7A). At this time, the TRCDATA0-3 signal 518 is output in units of 4 bits from the least significant bit at the timing of packet 1 (Fig. 7F).

[0016] To execute a write instruction of 32-bit data "5A5A5A5AH" to the address "001000H", the microcomputer 500 performs the following processing.

[0017] III) The CPU core 502 fetches a data write instruction from the address "000010H" in the internal memory, and executes the instruction. As a result, the CPU core 502 outputs the control signal 506 to the bus controller 503 and debugging controller 501. The control signal 506 instructs output of address data "000010H" to the external address bus 507 and output of write data "5A5A5A5AH" to the external data bus 508.

[0018] Note that the control signal 506 controls access to the memory in the microcomputer 500. Thus, even if the bus controller 503 receives the control signal 506, it does not output any data to the external address bus 507 and external data bus 508.

[0019] IV) In the debugging controller 501, the trace information generator 514, which has received the control signal 506, generates 40-bit trace data of format 3 (Fig. 6A), and outputs it to the trace information output unit 515. The trace information output unit 515, which has received the trace data, outputs trace data of format 3 (Fig. 6C) as the TRCDATAO-3 signal 518 (Figs. 8B to 8E) in synchronism with the leading edge of the CLKOUT signal 505 (Fig. 8A). At this time, the TRCDATAO-3 signal 518 is output in units of 4 bits from the least significant bit at the timing of packet 2' (Fig. 8F).

[0020] Since the conventional microcomputer outputs trace information by the above-described method, the debugging efficiency decreases in consecutive processing. This will be explained by exemplifying a case in which branch and data write instructions are consecutively executed.

[0021] In this consecutive processing, the microcomputer 500 executes processes I) to III). In this case, completing output of trace information for the branch instruction requires 10 clocks, as shown in Figs. 7A to 7F. However, most of the recent microcomputers operate in accordance with a branch instruction at nine clocks or less because of a high-speed operation request. Even if, therefore, the next write instruction is to be executed upon completion of the branch instruction, trace information for the branch instruction has not been completed yet.

[0022] The trace information generator 514 cannot perform process IV) until the trace information output unit 515 outputs all the trace information (buffer overflow). Thus, in consecutive processing, the trace information generator 514 generates pseudo trace information represented by format 1 in Fig. 6A, and sends the information to the trace information output unit 515. The trace information output unit 515 outputs the pseudo trace information in units of 4 bits from the least significant bit at the timing of packet 2 shown in Fig. 7F.

[0023] As described above, in the conventional microcomputer incorporating the on-chip debugging function, output of trace information cannot catch up with the processing speed during consecutive processing. For this reason, only pseudo trace information is output, debugging information runs short, and the debugging efficiency decreases.

[0024] The microcomputer incorporating the debugging function suffers the above problems because the real chip function is the main, and the number of trace buffers or trace information output terminals cannot be increased.

Summary of the Invention

[0025] It is an object of the present invention to provide a microcomputer capable of increasing the debugging efficiency.

[0026] To achieve the above object, according to the present invention, there is provided a microcomputer comprising an internal memory storing a control program, a CPU (Central Processing Unit) core for executing the control program stored in the internal memory, the CPU core outputting a control signal made up of connection information containing a storage address of the control program in the internal memory and an address of the internal memory generated as a result of executing the control program, instruction contents of the control program, and data generated by executing the control program, bus control means for controlling signal exchange based on an operation of the CPU core via an address bus and a data bus that are connected to an external memory, the bus control means having data I/O control means for, when the control signal is received from the CPU core, outputting an address obtained from the connection information in the control signal to the external address bus, and outputting the data in the control signal to the external data bus, and debugging control means for generating trace information necessary for debugging operation for confirming an operation by the control program, the debugging control means having trace information generation means for extracting the instruction contents in the control signal as trace information when the control signal is received from the CPU core, and trace information output means for externally outputting the trace information output from the trace information generation means.

Brief Description of the Drawings

[0027]

Fig. 1 is a block diagram showing the arrangement of the main part of a microcomputer according to the first embodiment of the present invention;

Figs. 2A to 2C are views each showing the trace packet format of trace information used in the microcomputer shown in Fig. 1;

Figs. 3A to 3H are timing charts in executing write and branch instructions by the microcomputer shown in Fig. 1;

Fig. 4 is a block diagram showing the arrangement of the main part of a microcomputer according to the second embodiment of the present invention;

Fig. 5 is a block diagram showing the arrangement of the main part of a conventional microcomputer;

Figs. 6A to 6C are views each showing the trace packet format of trace information used in the conventional microcomputer shown in Fig. 5;

Figs. 7A to 7F are timing charts in executing a branch instruction by the conventional microcom-

puter shown in Fig. 5; and
Figs. 8A to 8F are timing charts in executing a write instruction by the conventional microcomputer shown in Fig. 5.

Description of the Preferred Embodiments

[0028] The present invention will be described in detail below with reference to the accompanying drawings.

First Embodiment

[0029] A microcomputer according to the first embodiment of the present invention will be described. As shown in Fig. 1, a microcomputer 100 is constituted by a debugging controller 101, CPU core 102, bus controller 103, and internal memory 120.

[0030] The CPU core 102 performs control of generating and outputting a CLKOUT signal 105, and processing of executing various instructions and outputting a branch destination address value as a control signal 106 in executing a branch instruction. The internal memory 120 stores control programs executed by the CPU core 102.

[0031] The bus controller 103 comprises a data I/O controller 112 for exchanging an address value with an external address bus 107 and exchanging data with an external data bus 108 on the basis of the control signal 106 from the CPU core 102, and a priority processing controller 113 for instructing priority processing based on a predetermined priority when trace information output processing and access processing to an external memory (not shown) collide with each other. The bus controller 103 performs processing of outputting an active-high write signal MWR 109 to the external memory (not shown).

[0032] The debugging controller 101 comprises a trace information generator 110 for generating trace information in accordance with the control signal 106, and a trace information output unit 111 for outputting the trace information output from the trace information generator 110 as a TRCDATA0-3 signal 104 in time division.

[0033] When the access timing to the external memory (not shown) coincides with the debugging information output timing, the microcomputer 100 gives priority to output of debugging information. This priority processing control is done by the priority processing controller 113 of the bus controller 103. The priority processing controller 113 instructs the debugging controller 101 and data I/O controller 112 to perform priority processing. In this case, the priority processing controller 113 may instruct only a controller which performs lower-priority processing, i.e., the data I/O controller 112 to suspend the processing.

[0034] The trace information generator 110 generates trace information of a trace buffer overflow when the generator 110 receives the control signal 106 from the CPU core 102 as a result of executing a next instruction before the trace information output unit 111 outputs all trace information as the TRCDATA0-3 signal 104.

[0035] A trace packet format used in the microcomputer 100 having this arrangement will be described with reference to Figs. 2A to 2C.

[0036] In this embodiment, every trace packet is made up of 8 bits. Lower four bits represent trace information. As shown by formats 1 to 3 in Figs. 2A to 2C, "0011" represents the overflow of the trace buffer, "0110" represents execution of a branch instruction, and "1001" represents execution of data access.

[0037] Upper four bits in format 1 of Fig. 2A are fixed to "0000", and upper four bits in format 2 of Fig. 2B represent the type of branch instruction. In this embodiment, when an unconditional branch instruction is executed, "0100" is output. Bits 06 to 04 in format 3 of Fig. 2C represent the data access size, and "111" represents that access to one word (32 bits) has been executed. Bit 07 is fixed to "0".

[0038] Trace information output operation by the debugging controller 501 when branch and write are consecutively executed will be described.

[0039] The branch instruction is located at an address "000000H" in the internal memory 120 of the microcomputer 100, and is a branch instruction to an address "000010H". The write instruction is located at an address "000010H" in the internal memory 120, and a write instruction of writing 32-bit data "5A5A5A5AH" at an address "001000H". In the following description, the address bus width is 24 bits, the data bus width is 32 bits, and the trace buffer is made up of 4 bits equal in number to the terminals of the trace information output.

[0040] To execute a branch instruction to the address "000010H" that is located at the address "000000H" in the internal memory 120, the microcomputer 100 performs processing in the following order.

[0041] I) The CPU core 102 fetches the branch instruction from the address "000000H" in the internal memory 120, and executes the instruction. Then, the CPU core 102 outputs, to the bus controller 103 and debugging controller 101, the control signal 106 instructing output of the branch source address "000000H" to the external address bus 107.

[0042] II) Upon reception of the control signal 106, the data I/O controller 112 of the bus controller 103 outputs the branch source address "00000000H" to the external address bus 107 at the timing of bus cycle 1 (Fig. 3H).

[0043] III) Upon reception of the control signal 106, the trace information generator 110 in the debugging controller 101 generates 8-bit trace data of format 2 (Fig. 2B), and outputs it to the trace information output unit 111. The trace information output unit 111, which has received the trace data, outputs trace data as the TRCDATA0-3 signal 104 (Figs. 3B to 3E). As the TRCDATA0-3 signal 104, a packet of format 2 (Fig. 2B) is output in units of 4 bits from the least significant bit at the timing of packet 1 in synchronism with the leading edge of the CLKOUT signal 105 (Fig. 3A).

[0044] Subsequently, write processing to an external memory (not shown) is done.

[0045] IV) The CPU core 102 fetches a data write instruction from the address "000010H" in the internal memory 120, and executes the instruction. The CPU core 102 outputs, to the bus controller 103 and debugging controller 101, the control signal 106 instructing output of address data "000010H" to the external address bus 107 and output of write data "5A5A5A5AH" to the external data bus 108.

[0046] V) Upon reception of the control signal 106, the data I/O controller 112 outputs a next signal at the timing of bus cycle 2 (Fig. 3H). The data I/O controller 112 outputs address data "000010H" (Fig. 3F) to the external address bus 107, and outputs write data "5A5A5A5AH" (Fig. 3G) to the external data bus 108. At this time, the data I/O controller 112 changes the MWR signal 109 to an inactive level "0".

[0047] VI) Upon reception of the control signal 106, the trace information generator 110 in the debugging controller 101 generates 8-bit trace data of format 3 (Fig. 2C), and outputs it to the trace information output unit 111. The trace information output unit 111, which has received the trace data, outputs trace data as the TRCDATA0-3 signal 104 (Figs. 3B to 3E). As the TRCDATA0-3 signal 104, a packet of format 3 (Fig. 2C) is output in units of 4 bits from the least significant bit at the timing of packet 2 in synchronism with the leading edge of the CLKOUT signal 105 (Fig. 3A).

[0048] As described above, according to the first embodiment, the debugging controller 101 does not perform the conventional operation of loading data on a PC trace bus or emulation/data trace bus into the trace buffer or outputting the TRCDATA0-3 signal in time division in outputting trace information. The bus controller 103 outputs, to the external address bus and external data bus, the address of an instruction executed by the CPU core 102, the address at which the branch destination and data are stored, a data destination address, or data.

[0049] The TRCDATA0-3 signal uses only a total of 8-bit packet data, as shown in Figs. 2A to 2C, which greatly reduces the number of overflows of the trace buffer, compared to the conventional microprocessor. As described above, the microcomputer need not incorporate any PC trace bus or emulation/data trace bus. Since the trace buffer requires only a small number of bits, e.g., 8 bits, trace information can be output with the same number of trace information output terminals as that of the conventional microcomputer.

Second Embodiment

[0050] The second embodiment of the present invention will be described. As shown in Fig. 4, a microcomputer 400 in this embodiment is constituted by a debugging controller 101, CPU core 102, bus controller 401, and internal memory 120. The debugging controller 101, CPU core 102, and internal memory 120 are identical to those in Fig. 1, and a description thereof will be omitted.

[0051] The bus controller 401 comprises a data I/O controller 402 and priority processing controller 403. The data I/O controller 402 exchanges an address value with an external address bus 107, and exchanges data with an external data bus 108 on the basis of a control signal 106 from the CPU core 102. In exchanging an address value and data, a write signal MWR 109 is output to an external memory (not shown).

[0052] The priority processing controller 403 performs control of preferentially executing write operation in the external memory (not shown). The MWR signal 109 is an active-high signal.

[0053] In the first embodiment, when processing of loading data from the external memory collides with processing of outputting trace information to the external address bus 107 and external data bus 108, the priority processing controller 113 controls to perform trace information priority processing. This impairs real-time execution.

[0054] In the second embodiment, when these two processes collide with each other, the priority processing controller 403 informs the debugging controller 101 and data I/O controller 402 that priority is given to write processing to the external memory (not shown). After write processing to the external memory (not shown) ends, the microcomputer performs the same processing as in executing a branch instruction and accessing the internal memory 120. Hence, real-time execution of the microcomputer 400 is not impaired.

[0055] As has been described above, according to the present invention, the debugging controller does not process any trace information, which greatly reduces the number of overflows of the trace buffer used in the debugging controller, compared to the conventional microprocessor. Consequently, the debugging efficiency in the microcomputer incorporating the debugging function can increase.

[0056] Unlike the conventional microcomputer, the microcomputer need not incorporate any PC trace bus or emulation/data trace bus for connecting the bus controller and debugging controller. The microcomputer can be more simplified.

Claims

1. A microcomputer characterized by comprising:

   an internal memory (120) storing a control program;
   a CPU (Central Processing Unit) core (102) for executing the control program stored in said internal memory, said CPU core outputting a control signal made up of connection information containing a storage address of the control program in said internal memory and an address of said internal memory generated as a result

of executing the control program, instruction contents of the control program, and data generated by executing the control program;
bus control means (103, 401) for controlling signal exchange based on an operation of said CPU core via an address bus and a data bus that are connected to an external memory, said bus control means having data I/O control means (112) for, when the control signal is received from said CPU core, outputting an address obtained from the connection information in the control signal to the external address bus, and outputting the data in the control signal to the external data bus; and
debugging control means (101) for generating trace information necessary for debugging operation for confirming an operation by the control program, said debugging control means having trace information generation means (110) for extracting the instruction contents in the control signal as trace information when the control signal is received from said CPU core, and trace information output means (111) for externally outputting the trace information output from said trace information generation means.

2. A microcomputer according to claim 1, wherein said bus control means (103) comprises priority processing control means (113) for preferentially performing trace information output processing when trace information output processing by said debugging control means collides with signal exchange processing with the external memory by said data I/O control means.

3. A microcomputer according to claim 1, wherein said priority processing control means instructs at least said data I/O control means to suspend signal exchange processing with the external memory when two processes collide with each other.

4. A microcomputer according to claim 1, wherein said bus control means (401) comprises priority processing control means (403) for preferentially performing signal exchange with the external memory when trace information output by said debugging control means collides with signal exchange with the external memory by said data I/O control means.

5. A microcomputer according to claim 4, wherein said priority processing control means instructs at least said debugging control means to suspend trace information output processing when two processes collide with each other.

6. A microcomputer according to claim 1, wherein the trace information is made up of an 8-bit signal.

7. A microcomputer according to claim 1, wherein said bus control means outputs an active-high signal representing effective write to the external memory in outputting an address and data to the external address bus and the external data bus, respectively.

8. A microcomputer according to claim 1, further comprising any combination of the features set forth in claims 2 to 7.

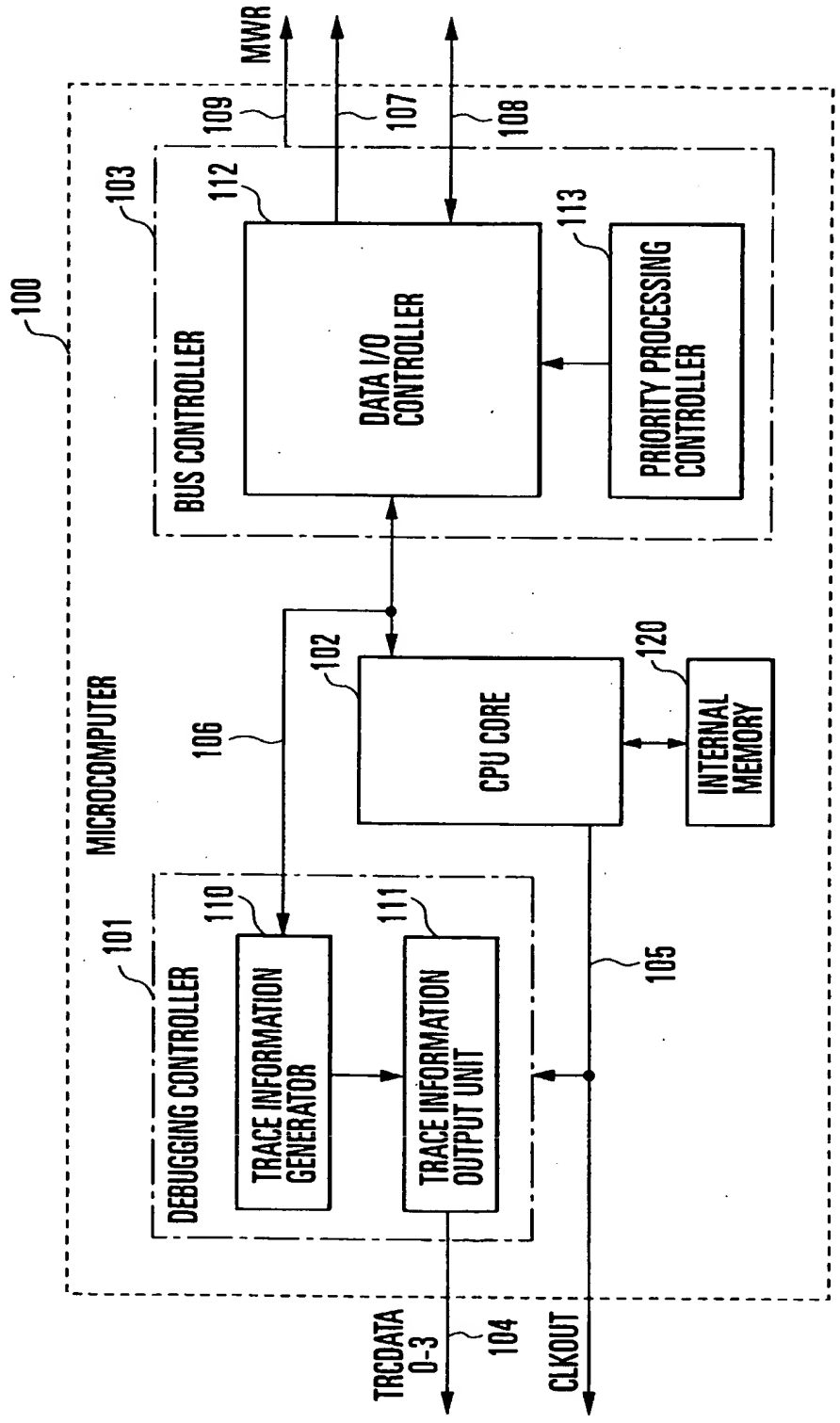
MWR
109
107
108
103
112
113
100
BUS CONTROLLER
DATA I/O CONTROLLER
PRIORITY PROCESSING CONTROLLER
MICROCOMPUTER
102
120
106
CPU CORE
INTERNAL MEMORY
101
110
111
105
DEBUGGING CONTROLLER
TRACE INFORMATION GENERATOR
TRACE INFORMATION OUTPUT UNIT
TRCDATA 0-3
104
CLKOUT

FIG. 1

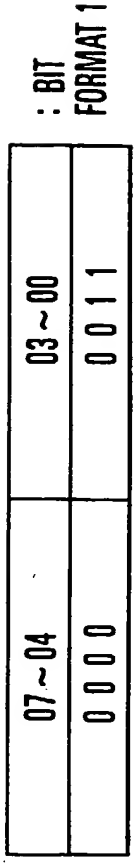

FIG. 2A

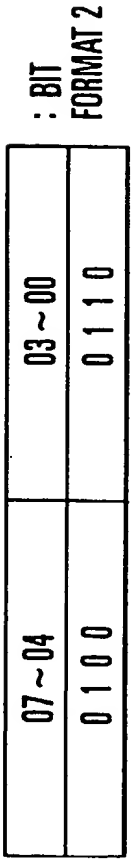

FIG. 2B

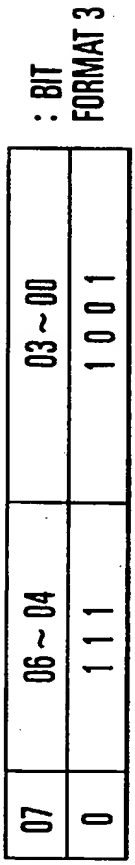

FIG. 2C

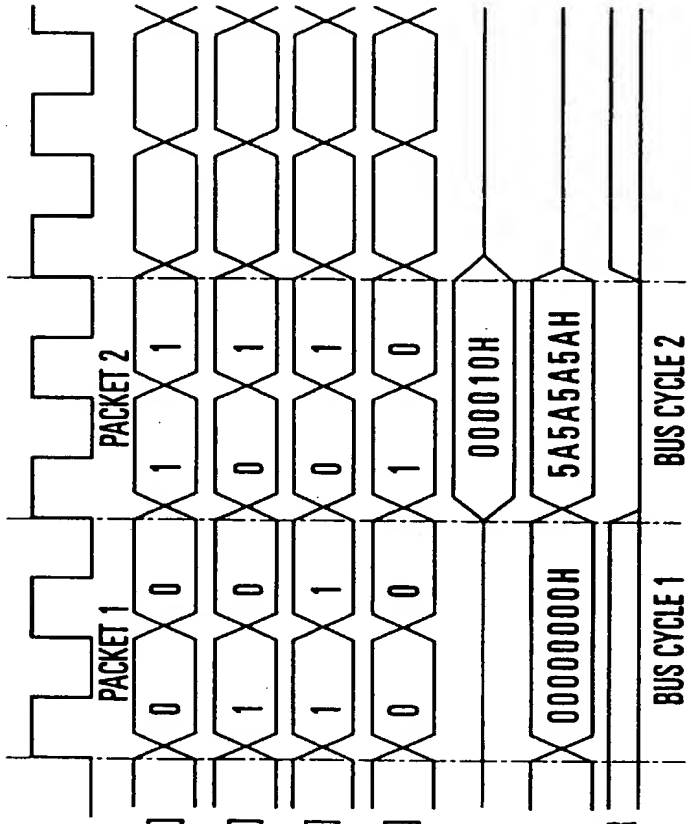

FIG.3A

FIG.3B

FIG.3C

FIG.3D

FIG.3E

FIG.3F

FIG.3G

FIG.3H

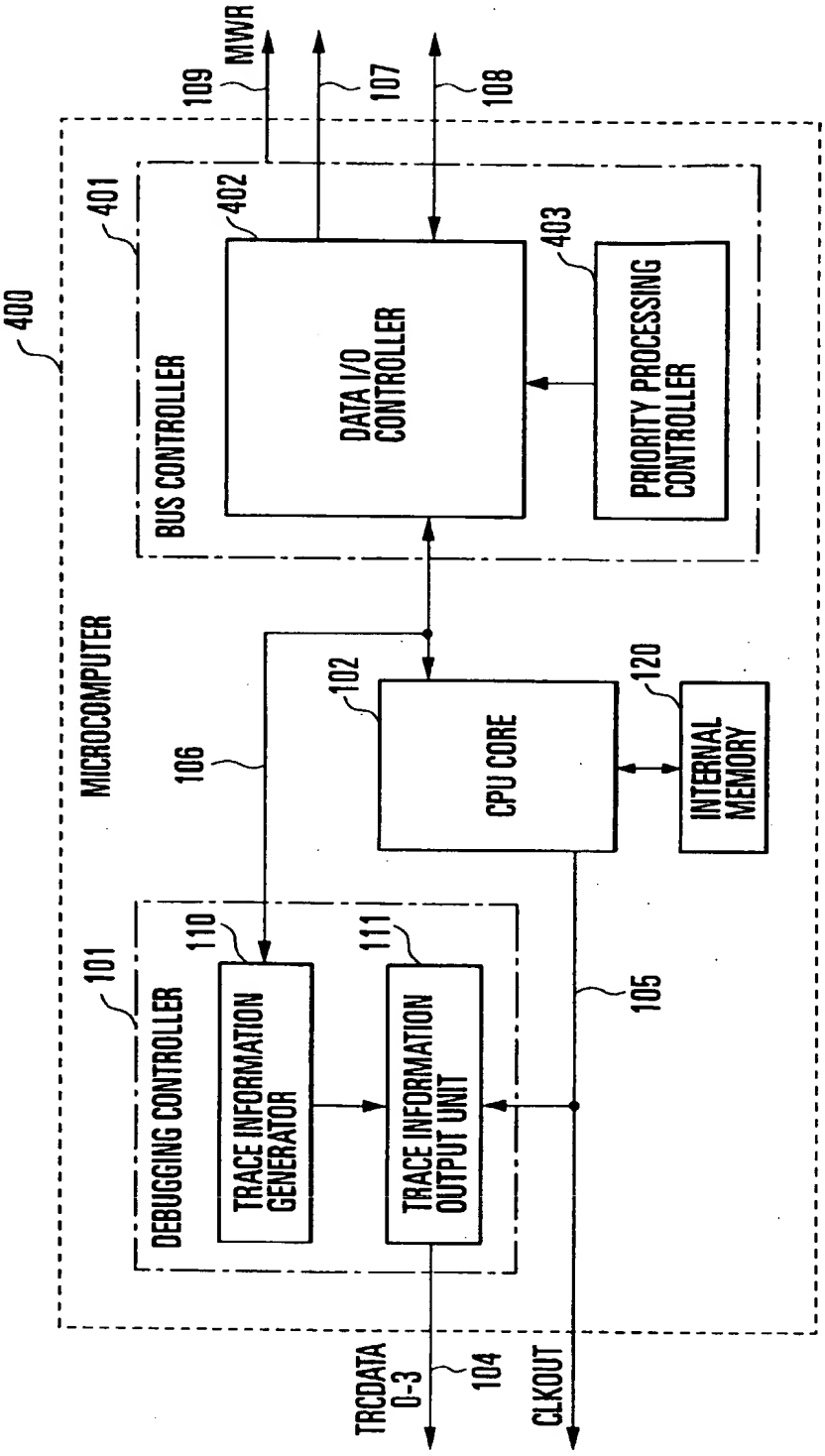
400
MICROCOMPUTER
401
BUS CONTROLLER
402
DATA I/O CONTROLLER
403
PRIORITY PROCESSING CONTROLLER
109
MWR
107
108
102
CPU CORE
120
INTERNAL MEMORY
106
101
DEBUGGING CONTROLLER
110
TRACE INFORMATION GENERATOR
111
TRACE INFORMATION OUTPUT UNIT
105
TRCDATA 0-3
104
CLKOUT

FIG. 4

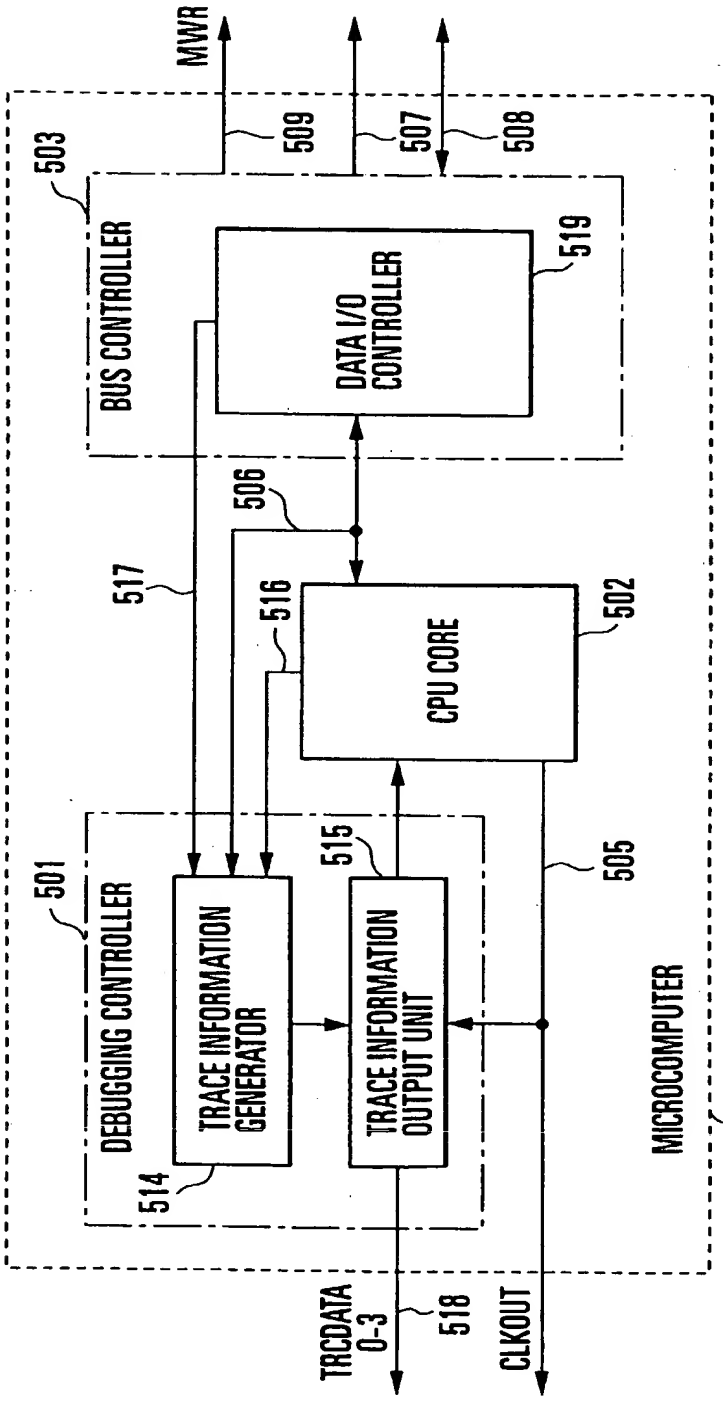

FIG. 5
PRIOR ART

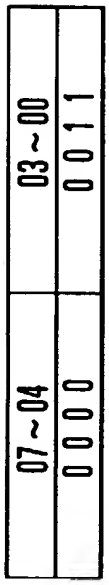

FIG. 6A

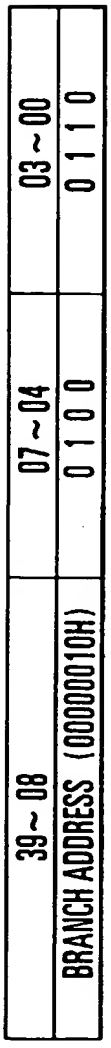

FIG. 6B

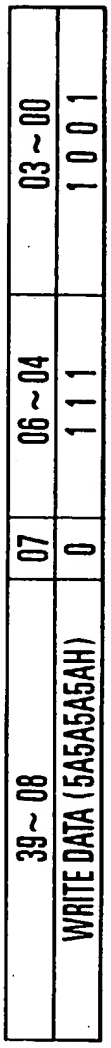

FIG. 6C

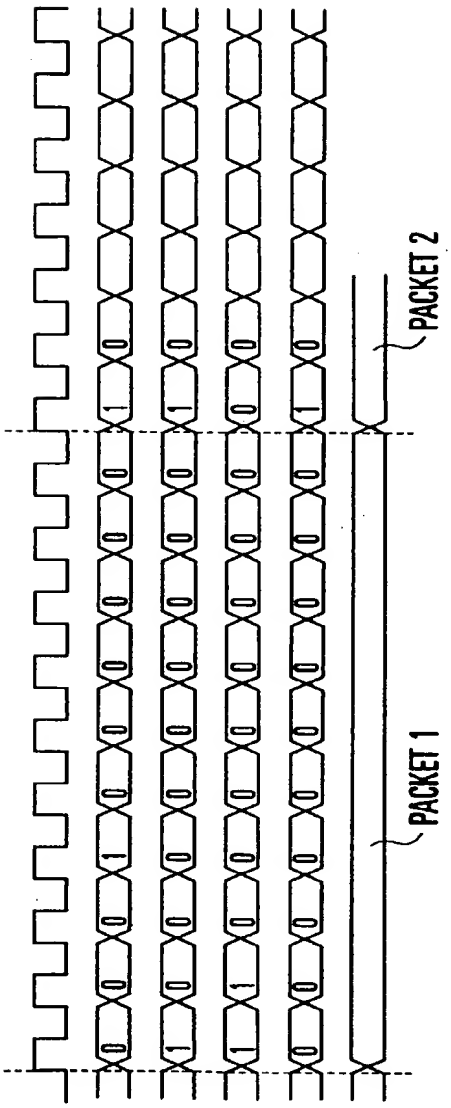

FIG. 7A
FIG. 7B
FIG. 7C
FIG. 7D
FIG. 7E
FIG. 7F

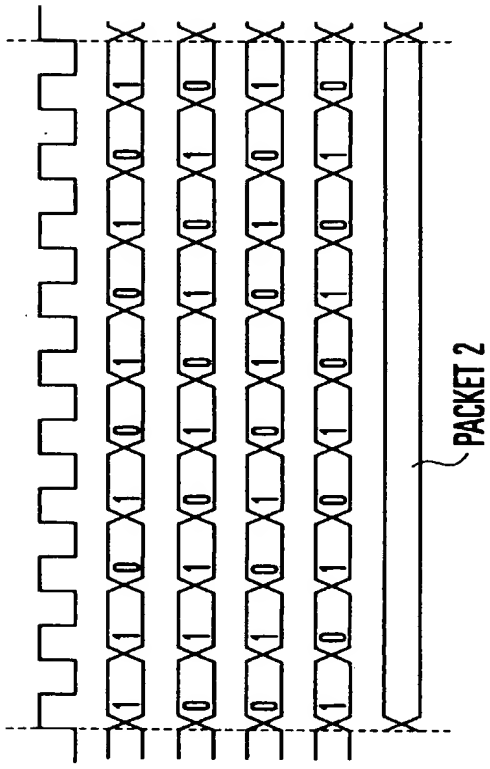

FIG. 8A
FIG. 8B
FIG. 8C
FIG. 8D
FIG. 8E
FIG. 8F